Remarks

Claims 1-3, 5-13, 22, 26-33, 35-37, and 45-56 are pending in the application, with claims 1, 22, 31, and 45 being the independent claims.

Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections Under 35 U.S.C. § 103

The Examiner argues that claims 1-3, 5-13, 22, 26-33, 35-37, and 45-56 are obvious and therefore unpatentable over U.S. Pat. No. 5,862,066 to Rossin *et al.* (hereinafter, "Rossin") in view of U.S. Pat. No. 6,115,047 to Deering (hereinafter, "Deering") and "A Programmable Pipeline for Graphics Hardware," PhD Dissertation, Department of Computer Science, University of North Carolina, Chapel Hill, April 1998 (hereinafter, "Olano"). Applicants respectfully traverse this rejection. Even if these references are combined for the sake of argument, such a combination still does not teach or suggest the claimed invention. Neither Rossin, Olano, nor Deering, taken alone or in combination, teaches or suggests the invention as recited in any of the pending claims.

In particular, the Examiner has rejected claim 1, arguing that this claim is rendered obvious by Rossin in view of Deering and Olano. In particular, the Examiner argues that Rossin discloses a rasterization circuit coupled to the processor that rasterizes a primitive according to a rasterization process which operates using a floating point format.

Rossin does not disclose this feature. The Examiner points to col. 3, lines 1-19 and col. 7, lines 18-41 of this reference, which discuss a graphics accelerator where division

operations are performed (see also FIG. 3 and col. 5, lines 23-25 and 28-31). Rasterization, however, is performed in a frame buffer subsystem (col. 2, lines 59-61), using the output of the graphics accelerator as input (col. 2, lines 32-35). This data, however, is converted from floating point to fixed point format before being sent to the frame buffer for rasterization (col. 4, lines 34-39). Therefore, Rossin discloses rasterization using fixed point data, not floating point data. Rossin does not disclose the feature of a rasterization circuit that rasterizes a primitive according to a rasterization process which operates using a floating point format.

The Examiner also argues that Deering discloses this feature, citing col. 9, lines 50-67 and col. 10, lines 1-50 of this reference. This passage discusses several components of a draw processor, but does not disclose a rasterization circuit that rasterizes a primitive according to a rasterization process which operates using a floating point format. While Deering does disclose floating point processors that perform certain operations, there is no disclosure of a rasterization circuit that rasterizes a primitive according to a rasterization process which operates using a floating point format.

For at least these reasons, claim 1 is not obvious over the Rossin, Deering, and Olano references when considered either alone or in combination.

The Examiner also argues that claims 2-13 are obvious in light of various combinations of Rossin, Olano, and Deering. The rejection of these claims is premised on the Examiner's above argument that claim 1 is obvious over Rossin, Deering and Olano. Claims 2-13 depend from claim 1 and therefore include all features of claim 1, including the feature of a rasterization circuit that rasterizes a primitive according to a rasterization process which operates using a floating point format. Given that this feature is not disclosed in

Deering, Olano, or Rossin, claims 2-13 are not rendered obvious over any of these references, whether considered alone or in combination.

The Examiner has also rejected claim 22 as being obvious over by Rossin in view of Deering and Olano, applying the same argument used in rejecting claim 1. For the reasons above, the cited references do not disclose or suggest claim 22's step of rasterizing data in a floating point format. For at least this reason, claim 22 is not rendered obvious by these references when considered either alone or in combination.

The Examiner also argues that claim 26, which depends from claim 22, is obvious over Rossin in light of Olano and Deering. The Examiner has not addressed the patentability of claims 27-30, which also depend from claim 22, but presumably these claims are also rejected as obvious over various combinations of Rossin, Olano, and Deering. The rejection of claims 26-30 is premised on the Examiner's above argument that claim 22 is obvious over Rossin in view of Deering. Claims 26-30 depend from claim 22 and therefore include all steps of claim 22, including the step of rasterizing data in a floating point format. Given that this step is not disclosed in Deering, Olano, or Rossin, claims 26-30 are not rendered obvious over these references, whether considered alone or in combination.

The Examiner has also rejected independent claim 31 as being obvious over Rossin, Deering, and Olano. Here the Examiner contends that all three references disclose claim 31's feature of a raster subsystem for performing a rasterization process, the rasterization process performed in a floating point format. As discussed above with respect to claim 1, however, none of these references make this disclosure. Rossin discloses conversion of data into fixed point format prior to rasterization; Deering discusses rasterization but does not disclose performing rasterization in a floating point format; and Olano fails to teach a rasterization

process performed in a floating point format. For at least these reasons, claim 31 is not rendered obvious over these references, whether considered alone or in combination.

The Examiner also argues that claims 32, 33, and 35-37 are obvious in light of various combinations of Rossin, Olano, and Deering. The rejection of these claims is premised on the Examiner's above argument that claim 31 is obvious over Rossin, Deering, and Olano. Claims 32, 33, and 35-37 depend from claim 31 and therefore include all features of claim 31, including the feature of a raster subsystem for performing a rasterization process, the rasterization process performed in a floating point format. Given that this feature is not disclosed in Deering, Olano, or Rossin, claims 32, 33, and 35-37 are not rendered obvious over any of these references, whether considered alone or in combination.

The Examiner has also rejected claim 45 for the same reasons as claim 1, arguing that this claim is rendered obvious by Rossin in view of Deering and Olano. In particular, the Examiner argues that Rossin discloses a rasterization module coupled to a processor that rasterizes the primitive according to a rasterization process which operates using a floating point format. As stated above with respect to claim 1, none of Rossin, Deering, or Olano discloses this feature. For at least this reason, claim 45 is not obvious over the Rossin, Deering, and Olano references when considered alone or in combination

The Examiner also argues that claims 46-56 are obvious in light of various combinations of Rossin, Olano, and Deering. The rejection of these claims is premised on the Examiner's above argument that claim 45 is obvious in view of these references. Claims 46-56 depend from claim 45 and therefore include all features of claim 45, including the feature of a rasterization module coupled to a processor that rasterizes the primitive according to a rasterization process which operates using a floating point format. Given that this feature

is not disclosed in Deering, Olano, or Rossin, claims 46-56 are not rendered obvious over any of these references, whether considered alone or in combination.

Moreover, Applicants wish to point out that the Deering reference, U.S. Patent No. 6,115,047, has a filing date of March 18, 1998. Applicants, however, conceived of the invention prior to this date. Applicants can, if necessary, provide a declaration under 37 CFR § 1.131 along with supporting documentation regarding the invention date of the present invention. Such a declaration would establish invention of the subject matter of the rejected claims prior to the effective date of the Deering reference, coupled with due diligence from the date of conception to the effective filing date of the present application.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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